

PATENT NUMBER

**U.S. UTILITY Patent Application**

mH O.I.P.E.  
 SCANNED TR3 Q.A. Ed

**PATENT DATE**

APPLICATION NO. 09/924318	CONT/PRIOR	CLASS 438	SUBCLASS	ART UNIT 1765	EXAMINER Tran, B
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Method of building a CMOS structure on thin SOI with source/drain electrodes formed by in situ doped selective amorphous silicon

PTO-2040  
12/99

<b>ISSUING CLASSIFICATION</b>								
<b>ORIGINAL</b>		<b>CROSS REFERENCE(S)</b>						
<b>CLASS</b>	<b>SUBCLASS</b>	<b>CLASS</b>	<b>SUBCLASS (ONE SUBCLASS PER BLOCK)</b>					
<b>INTERNATIONAL CLASSIFICATION</b>								

☐ Continued on Issue Slip Inside File Jacket

 <b>TERMINAL DISCLAIMER</b>	<b>DRAWINGS</b>		<b>CLAIMS ALLOWED</b>	
	Sheets Drwg.	Figs. Drwg.	Print Fig.	Total Claims
<input type="checkbox"/> The term of this patent subsequent to _____ (date) has been disclaimed.	_____ (Assistant Examiner)		<b>NOTICE OF ALLOWANCE MAILED</b>	
<input type="checkbox"/> The term of this patent shall not extend beyond the expiration date of U.S. Patent. No. _____	_____ (Primary Examiner)		<b>ISSUE FEE</b>	
			Amount Due	Date Paid
<input type="checkbox"/> The terminal _____ months of this patent have been disclaimed.	_____ (Legal Instruments Examiner)		<b>ISSUE BATCH NUMBER</b>	

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